

Macrocad Development Inc. VSM 8014 I2C Simulation Models

Description:

Macrocad's VSM 8014 models are behavior models for creating a virtual reality system simulation environment based on the I2C bus specifications. System developers will appreciate the ease of use, and features which allow the designer to manipulate the system at will. Each model is an independent agent - there are no interdependencies to constrain the designer, or to make the system artificial in its operation. Operating parameters are passed to each model to characterize their behavior. Master models execute an instruction list so I2C transaction sequences are easy to control. Simulations run in batch and interactive modes.

Features:

- ◇ Independent agents - realistic system simulation
- ◇ Function and timing checks are automated
- ◇ All I2C transactions are logged
- ◇ Master operates from an instruction list
- ◇ I2C bus sequences are easily controlled
- ◇ Designed *by* hardware engineers *for* hardware engineers
- ◇ System Backbone and Test Bench Included
- ◇ Master, Slave, Log, and Timing Check Models
- ◇ I2C 10 bit addressing supported
- ◇ 100KHz and 400KHz I2C speeds supported
- ◇ High Speed option supported

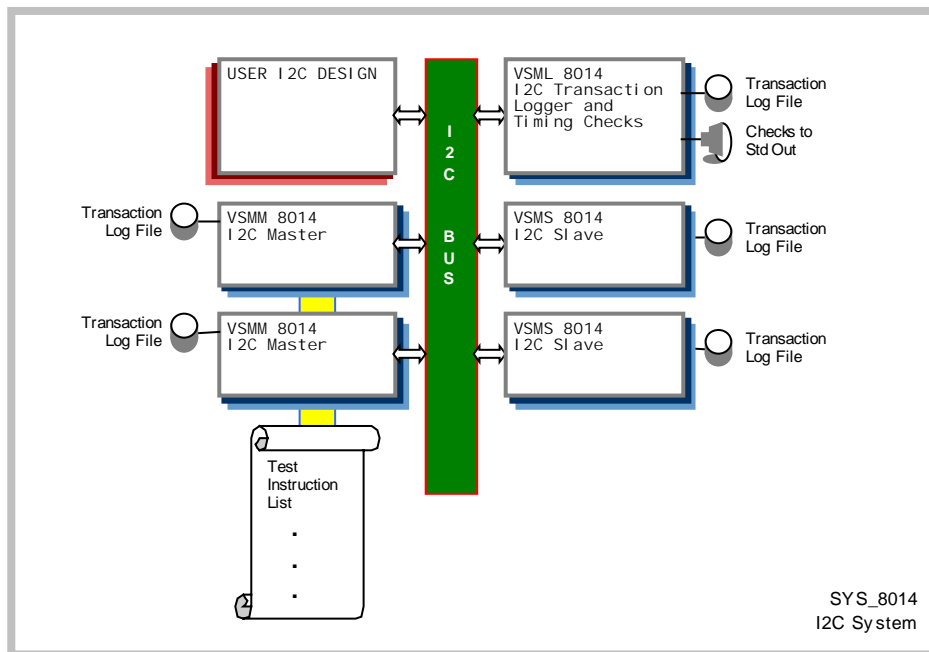


Figure 1

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System Architecture

System Operation

The simulation acts like a real I2C based serial communications system. The masters follow an instruction list contained in the SYS_8014 module. The slaves are memory devices, and respond, when accessed within their address range, as determined by operating parameters. The checker model

reports on functional and timing violations, and logs all I2C transactions. Each model is individually selectable for speed (100KHz, 400KHz, or High Speed), device address (for slaves), and several debugging and data logging features.

SYS_8014 I2C System Model

This model is the system backbone for I2C based system simulation environments. All I2C devices, structural or behavioral “plug” in to this backbone. A variety of masters and slaves can be assembled on this system backbone, as well as user designs. This level also contains the instruction. This instruction list initiates operations in the master models instantiated at this level. In this way, several masters can be controlled by the same instruction sequence. Any number of slaves and masters can be instantiated. Each model can be characterized for its operation. Parameters such as speed, device

address, addressing mode (7 or 10 bit), log file name, and debug switches, are all set individually for each model at this level. Debug features can be set at compile time for each instantiation of a model, and they can also be switched on and off during simulation run time. All transactions are sequence stamped, so that when comparing master and slave log files, the specific transaction can be isolated in each master, slave and I2C transaction log file. The master and the slave log all start and stop events which the sequence stamp, but only log data transactions which they participate in.

VSMS8014 I2C Slave Model

The VSMS8014 slave model acts as a memory slave on the I2C bus. It supports fast, normal, and high speed I2C transactions, as well as slower speeds. It drives the bus with worst case timing assumed.

Device address, memory location (address) and data transfers are all tracked, reported, and logged. Each I2C frame is tracked, and the sequence number is tracked, reported and logged.

VSMM8014 I2C Master Model

The VSMM8014 I2C master model initiates I2C transactions. It follows an instruction list contained at the system level. It supports 10 and 7 bit addressing, fast, normal and high speed I2C speeds, and multi

mastering arbitration. For example, when instructed, this model will execute an I2C start operation. It will execute the next instruction in the list, which could be a data transaction, or a stop, etc. If in the

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process of a transaction, if there is another master driving the SDA line, the I2C multi-mastering arbitration scheme will determine the 'winner'. If the master does not win the arbitration, then it will stop driving the bus signals, (both clock and data, SCL and SDA). Debug

messaging, and 'stop on error' features are selectable. Stop on error is selectable with each new instruction. Data transaction logging is selectable, as well as reporting on data transaction errors, lost arbitration, and correctly and misplaced start and stop events.

VSML8014 I2C Logger / Checker Model

The VCML8014 logger model tracks all I2C activity. Like the slave and master models, it tracks sequential frames and reports and logs this information for correlating log file information. Since it does not participate in I2C transactions, it does not drive either SCL or SDA. It

checks for functional violations, and has an I2C timing checker included. The timing checker monitors SCL, SDA, SCLH, and SDAH activity to determine timing violations for both fast, normal, and high speeds. These violation are reported to the Std Out.

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System Test Creation and Execution

In order to construct a test which involves the participation of several models, each model must be properly configured, and 'set up' at the system level. Once the models are configured, the transactions specified must be consistent with the test objective. Tests can be constructed to verify the ability to

handle all normal data transactions to a specific I2C device. Tests can also be constructed to verify that a specific I2C device handles error conditions properly. The test is determined by the list of transaction instructions which are executed by the VSMM8014 master/driver model.

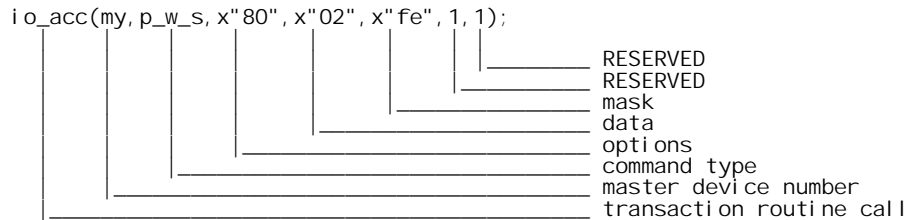


Figure 2

Figure 2 shows a typical access for an I2C transaction. In this case, it results in master device 4, (my = 4) executing an I2C start operation followed by an I2C write with I2C data of 0x04. In this case, since

option bit 0 is 0, it will check to see that the ack bit is a 0, (slave device select acknowledge). The slave address is shifted from 0x02 to 0x04 with the write bit taking the bit 0 position.

VALID COMMANDS ARE:

- p_rs : reset
- p_sl : RESERVED
- p_rd : read from I2C core
- p_wr : write to I2C core
- p_x_s : start I2C frame with data presented
- p_w_s : start I2C frame WRITE with address = data 7:1
- p_r_s : start I2C frame READ with address = data 7:1
- p_w_d : write I2C data byte
- p_r_d : read I2C data byte
- p_x_p : stop I2C frame
- p_x_i : interrupt the high speed bus frame
- p_x_f : change the I2C speed factor

OPTION BIT DEFINITIONS ARE:

- bit 7:1 : timeout value for starting I2C activity
- bit 0 : generate ACK bit on reads, and check for ACK bit on writes

Figure 3

Figure 3 lists the valid commands for VSMM8014 master operations. It also lists the option definition. The read and write

from I2C core calls are not included, and should be provided by the user.

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Model Configuration

Operational parameter information can be entered as constants at the system (SYS_8014) level. These

constants include the file names and paths for log files, etc.

Model	Constant Name	Range	Type	Definition
VSMM8014	p_dev		integer	Device number
	p_split		integer	Split high/speed and normal/fast I2C bus
	p_debug_level	15:0	vector	Debug switches
	p_log_enable		integer	Enable transaction logging
VSMS8014	p_dev		integer	Device number
	p_split		integer	Split high/speed and normal/fast I2C bus
	p_debug_level	15:0	vector	Debug switches
	p_log_enable		integer	Enable transaction logging
VSML8014	p_split		integer	Split high/speed and normal/fast I2C bus
	p_debug_level	15:0	vector	Debug switches
	p_log_enable		integer	Enable transaction logging
	p_log_file_name		string	Log file path and name
SYS_8014	VERSION	31:0	Vector	Model version indication
	p_debug_level	15:0	Vector	Debug switches
	p_test_mask	15:0	Vector	Test selection
	p_2_addr_7	6:0	Vector	Device 2 7 bit address
	p_2_addr_10	9:0	Vector	Device 3 10 bit address
	p_5_addr_7	6:0	Vector	Device 5 7 bit address
	p_5_addr_10	9:0	Vector	Device 5 10 bit address
	p_split		integer	Split high/speed and normal/fast I2C bus
	mx		Integer	Device 1 mnemonic
	my		Integer	Device 4 mnemonic

These parameters can be set to unique values for each instantiated

model. These are to be considered constants.

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Model Operational Handshake

Model	Port Name	Range	Type	Definition
VSMM8014				
	sdah	Scaler	Inout	High speed data
	sclh	Scaler	Inout	High speed clock
	sda	Scaler	Inout	Normal fast data
	scl	Scaler	Inout	Normal fast clock
	stat	7:0	Out	Return status
	retdata	7:0	Out	Return data
	data	7:0	In	Request data
	addr	7:0	In	Request options
	ctrl	7:0	In	Request command type
	mask	7:0	In	Request data mask on reads
	loop_interval	7:0	In	RESERVED
	loop_limit	7:0	In	RESERVED
VSMS8014				
	sdah	Scaler	Inout	High speed data
	sclh	Scaler	Inout	High speed clock
	sda	Scaler	Inout	Normal fast data
	scl	Scaler	Inout	Normal fast clock
	p_addr_7	6:0	Vector	7 bit address
	p_addr_10	9:0	Vector	10 bit address
VSML8014				
	sdah	Scaler	Inout	High speed data
	sclh	Scaler	Inout	High speed clock
	sda	Scaler	Inout	Normal fast data
	scl	Scaler	Inout	Normal fast clock
	speed	7:0	In	Selects between fast and normal timing checks, <0x01 = fast, 0x00 = normal >

These ports are the I2C operation signals, and the transaction request and response for initiating I2C

operations. The slave also has I2C device address selection vectors.

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