Xbench for AMBA AHB

Synthesizable AHB Models from Macrocad Development Inc.

Benefits

High Performance

- Synthesizable AHB protocol for maximum acceleration and emulation performance

Software Controllability

- Easy to use transaction-level API provides maximum flexibility and controllability

Features

- Compliance with AMBA Specification 2.0
- Verilog modules integrate seamlessly into your current design environment
- Transaction level API Language binding for C, or command file
- Completely synthesizable AHB master, slave, arbiter, decoder, and multiplexor
- Non-preemptive multi-threaded programming environment with blocking and non-blocking functions capable of complex testbenches
- High-speed software/hardware communication mechanism capable of targetless emulation speed
- AHB tracker/logger for error detection and functional coverage
- Random transaction support

Functional Verification for AHB

AHB (Advanced High-performance Bus) is the latest generation AMBA (Advanced Microcontroller Bus Architecture) bus. It is intended to address the requirements of high-performance synthesizable designs. Many system-on-a-chip designs in the portable electronics, telecommunications, and embedded systems markets use AHB to interface application specific design blocks with standard microcontrollers from ARM Limited.

Testbench Automation

To verify designs containing an AHB, a transaction-based verification environment and high-level languages, such as C/C++, are often used to automate test generation. These languages provide the data structures, randomization, and synchronization features to make testbenches easier to write, debug, and maintain.

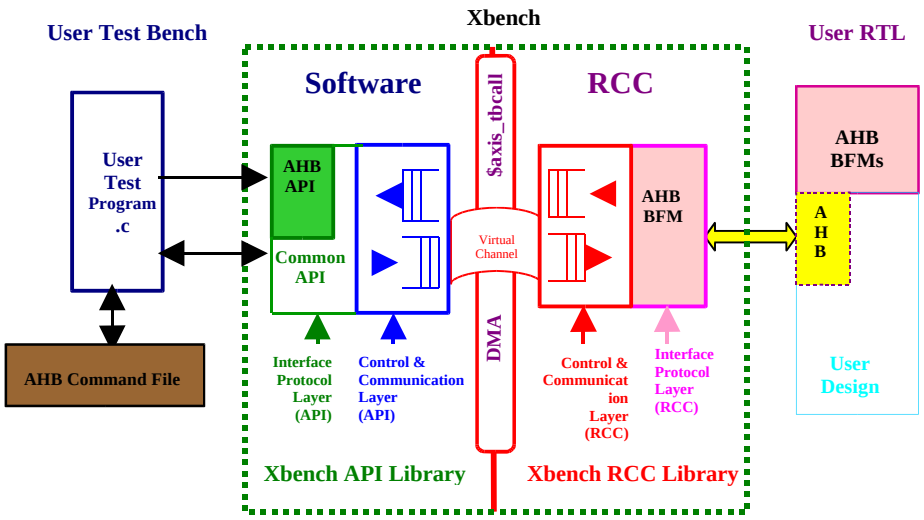
Performance

To achieve high performance levels to promptly verify designs containing an AHB requires simulation acceleration and emulation technologies. Traditionally, these technologies have required synthesizable testbenches.

Xbench for AMBA AHB

Xbench for AMBA AHB reconciles the seemingly conflicting requirements between the benefits of high-level languages and the performance offered by low-level testbenches, by providing an AHB verification environment that takes advantage of the benefits of high-level languages for testbench development and provides the highest performance levels for acceleration and emulation.

Macrocad Development, Inc. has partnered with Axis Systems, Inc. by providing synthesizable models of AHB components (Macrocad 5200 modules) and an AHB-specific API (applications



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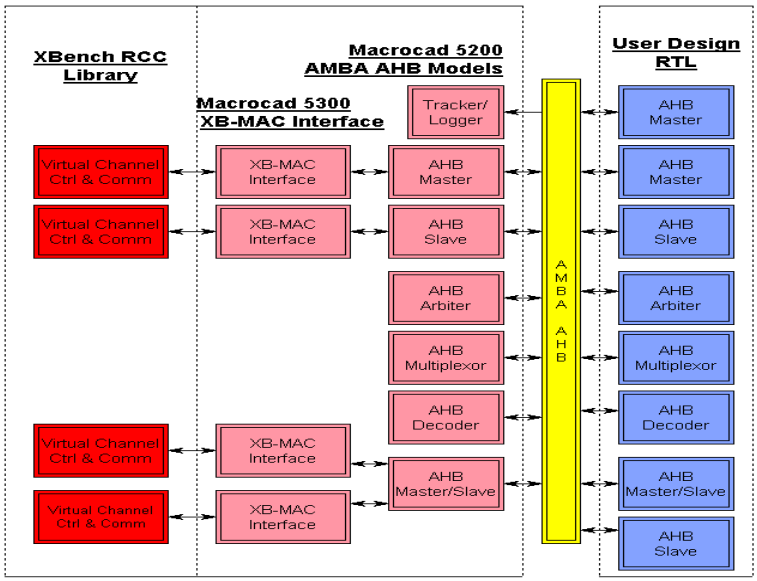
programming interface), integrated with the models at a transaction level through the Macrocad 5203 modules and Xbench from Axis Systems.



Test and Bench

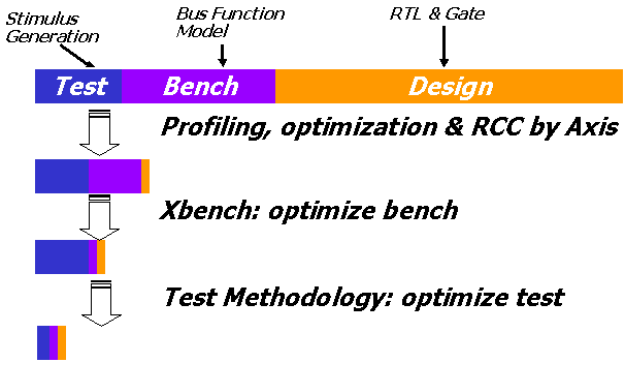
The Xbench for AMBA AHB architecture separates the transaction level API (test) from the synthesizable AHB protocol (bench), connecting them via a high-speed communication channel that does not transfer any primary inputs or outputs on each clock cycle of simulation. The result is an optimized bench that provides the fastest possible AHB verification environment with the same level of control commonly found in un-acceleratable behavioral AHB models. Xbench is the first verification tool that you can use during all phases of a project; it works well with software simulation, acceleration, and emulation.

Unify Your AHB Environment

Xbench for AMBA AHB unifies your verification environment by eliminating the need to change models and testbench languages between software simulation, acceleration, and emulation. Xbench provides a high-performance AHB interface optimized for Xcite and Xtreme hardware from Axis Systems.

Xbench for AMBA AHB Specifications

AHB Standard	AMBA Specification 2.0 (ARM IHI 0011A)
Supported Platforms	Sun Solaris, Red Hat Linux
Required Axis Component	XSIM, Xcite, Xtreme, Xbench
AHB Components	Master, Slave, Arbiter, Decoder, Multiplexor, Tracker, Logger
AHB Support **All AHB Transactions Supported**	Memory read/write Transaction pipelining Single and burst transfers 4, 8, and 16 beat incrementing and wrapping bursts Arbitrary length incrementing bursts up to 1024 bytes Split /retry transactions Multi-layer AHB capable Equal rotation priority bus arbiter
Controllability	Master and slave characteristics completely programmable Configurable slave Memory space Configurable wait state insertion
Constrained Randomness	Two-levels of constraints Random transaction generation Transaction coverage
Language Bindings	C/C++ Command File



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