Macrocad Development Inc.
VCM 8574 I2C Synthesizable Port Model

Description:

The VCM 8574 model from Macrocad is a synthesizable behavior HDL for creating a serial interface controller based on the I^2C bus specification. Implementations are made easy for both FPGAs and ASICs. Synchronous design and small module size assures worry free synthesis. Hierarchical state machine design is easily modified. Well commented code provides insight into operations. Digital filters to synchronize I^2C signals are programmable. Bi-directional signals are contained in the buffer (shell) level, the core contains unidirectional signals only.

Features:

- Synthesizable RTL HDL code
- Available in Verilog and VHDL versions
- Synchronous design
- Digital signal filtering
- Well commented code for clarity
- Test bench is included
- 100KHz and 400KHz supported
- 8 bit slave port
- Compatible with the PCF8574
- Designed *by* hardware engineers *for* hardware engineers
- Supports I2C Version 2.0 Spec.

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Architecture

The SHEL8574 is an I2C slave model capable of interfacing the I2C serial bus with an 8 bit parallel utility port. The top level is an optional bi-directional shell which contains the only bi-directional and tristate signals in the model. The core level contains the functional blocks and state machines for tracking and responding to the I2C serial traffic, and controlling the 8 bit utility port.

Pin List

Figure 2 shows the core8574 signal pins.

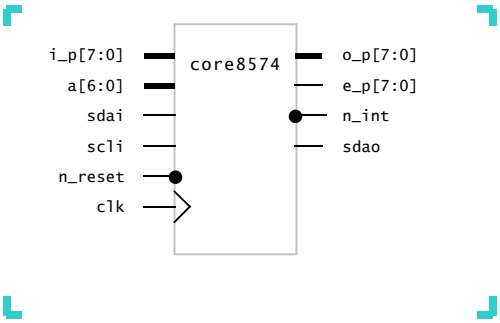

figure 2

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Table 1 lists the shel8574 and core8574 signal pins.

SHELL	CORE	TYPE	DESCRIPTION
p7		BI-DIRECT	Port bit 7
p6		BI-DIRECT	Port bit 6
p5		BI-DIRECT	Port bit 5
p4		BI-DIRECT	Port bit 4
p3		BI-DIRECT	Port bit 3
p2		BI-DIRECT	Port bit 2
p1		BI-DIRECT	Port bit 1
p0		BI-DIRECT	Port bit 0
	o_p [7:0]	OUT	Port output
	i_p [7:0]	IN	Port input
	e_p [7:0]	OUT	Port enable
n_int	n_int	OUT	Interrupt, pin change
sda		BI-DIRECT	i2c data
	sdao	OUT	i2c data output
	sdai	IN	i2c data input
scl		BI-DIRECT	i2c clock
	scli	IN	i2c clock input
a0[6:0]	a0[3:0]	IN	I2C Address selects
clk	clk	IN	Master clock
n_reset	n_reset	IN	Reset

table 1

Support Models:

The SYS_8574 model is the top level interconnect model. It contains a SHEL8574 I2C port expander slave, the test list to be executed, the VSMM8014 I2C master model, and the VSML8014 I2C bus transaction logger and timing checker. The SHEL8574 model responds to the I2C serial traffic. This traffic is generated by the VSMM8014 I2C master model. Stimulus for the VSMM8014 is provided by execution of the test instruction list. Each instruction in the test list specifies the device to be accessed as a part of a sequence of I2C instructions.

VSML8014 I2C transaction Logger Model

The I2C bus logger model tracks the I2C bus, both high/speed and normal/fast. All I2C bus transactions can be logged to a file. This feature is optional.

I2C timing is checked for normal, (default) or fast timing specifications. To check for fast timing, a select integer needs to be set to 1. This is the i_speed integer in the VSML8014 model. This integer is set to its default value at compile time, but can be changed thereafter.

High/Speed timing is checked without user intervention. The VSML8014 model tracks all I2C transactions, so it detects when high/speed mode is enabled and enables high speed timing checks. The VSML8014 model instantiates two separate models for these timing checks, one for normal/fast (VSMT8014) and one for high/speed, (VSMH8014).

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VSMM8014 I2C Master Model

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The VSMM8014 I2C master model initiates I2C transactions. It follows an instruction list contained at the system level. It supports 10 and 7 bit addressing, fast and normal I2C speeds, and multi mastering arbitration. For example. when instructed, this model will execute an I2C start operation. It will execute the next instruction in the list, which could be a data transaction, or a stop, etc. If in the process of a transaction, if there is another master driving the SDA line, the I2C multi mastering arbitration scheme will determine the 'winner'.

If the master does not win the arbitration, then it will stop driving the bus signals, (both clock and data, SCL and SDA). Debug messaging, and 'stop on error' features are selectable. Stop on error is selectable with each new instruction. Data transaction logging is selectable, as well as reporting on data transaction errors, lost arbitration, and correctly and misplaced start and stop events.

The formats for the request and acknowledge vectors are shown below.

VECTOR	RANGE	DESCRIPTION
Req	63:0	DRIVER REQUEST VECTOR
	63:56	Tag - request / response handshake
	55:48	Control - type of register access
	55:49	RESERVED
	48	1 : write
		0 : read
	47:40	Address
	47:44	RESERVED
	43:40	Address - register selects
	39:32	Data
	31:24	Mask - mask data bits
	23:16	Limit limit - upper limit on repeated accesses
	15:8	Loop interval - time between repeated access
	7:0	Check
	7:1	RESERVED
	0	1 : check for data errors
		0 : Ignore received data
Rsp	63:0	DRIVER RESPONSE VECTOR
	63:56	Tag - tag request plus 1
	55:48	Control <request mirrored>
	47:40	Address <request mirrored>
	39:32	Data on shel8574 data bus signal pins
	31:24	Mask <request mirrored>
	23:16	Limit limit <request mirrored>
	15:8	Loop interval <request mirrored>
	7:0	Check <request mirrored>

table 5

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