

Macrocad Development Inc. VCM8251 Synthesizable UART Model

Description:

The VCM 8251 model from Macrocad is a synthesizable behavior HDL for implementing an 82510 compatible UART function. Implementation is made easy for both FPGAs and ASICs. Synchronous design and small module size assures worry free synthesis. Well commented code provides insight into operations. Bi-directional signals are contained in the buffer (shell) level, the core contains unidirectional signals only. Noise immunity options improve reliability of serial communications. Dual buffers reduce overrun problems. Dual timer / baud rate generators provide flexible serial rate options. Optional edge syncing increases serial signal jitter immunity.

Features:

- ◇ Synthesizable RTL HDL code
- ◇ Modular design provides flexibility
- ◇ Synchronous design
- ◇ Test bench is included
- ◇ Buffers are expandable
- ◇ Compatible with 82510 UART
- ◇ Majority voting – noise immunity
- ◇ Optional resync on incoming serial edge
- ◇ Character or address recognition
- ◇ 9 bit and parity options
- ◇ 2 programmable timers / baud rate generators
- ◇ Automatic modem handshake option
- ◇ Dual port SRAM, or edge triggered register array used for FIFO function
- ◇ Available in Verilog and VHDL versions
- ◇ Less than 10k gates (asic gates)

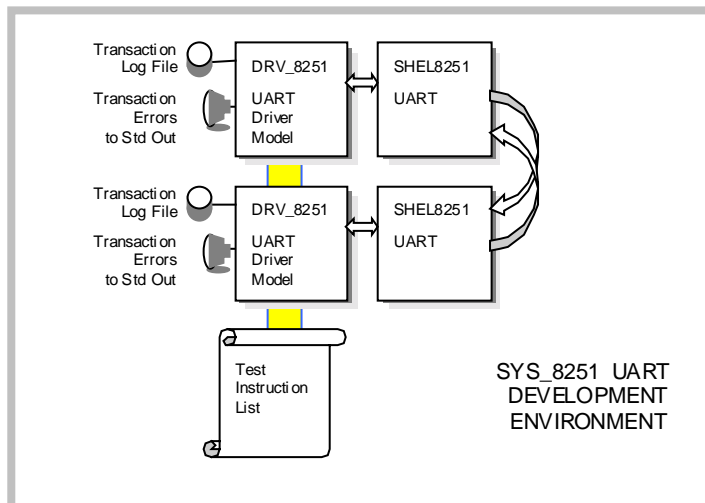


Figure 1

Figure 1 shows the test bench environment for the UART cores.

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Architecture

MacroCAD's VCM 8251 is a synthesizable 82510 compatible behavior model. This model provides the system designer with a drop in UART function. This model is functionally partitioned to provide the most flexibility for various ASIC and FPGA

implementations. It includes two data buffer memories for improved serial communications. The IO buffer shell level contains the bi-directional buffer I/O signals. The functional units are all contained in the core level.

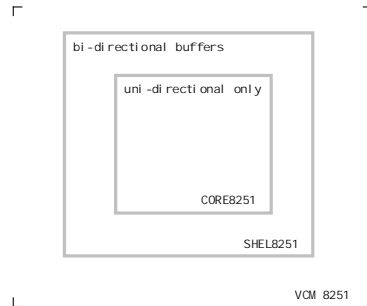


Figure 2

Core Pins

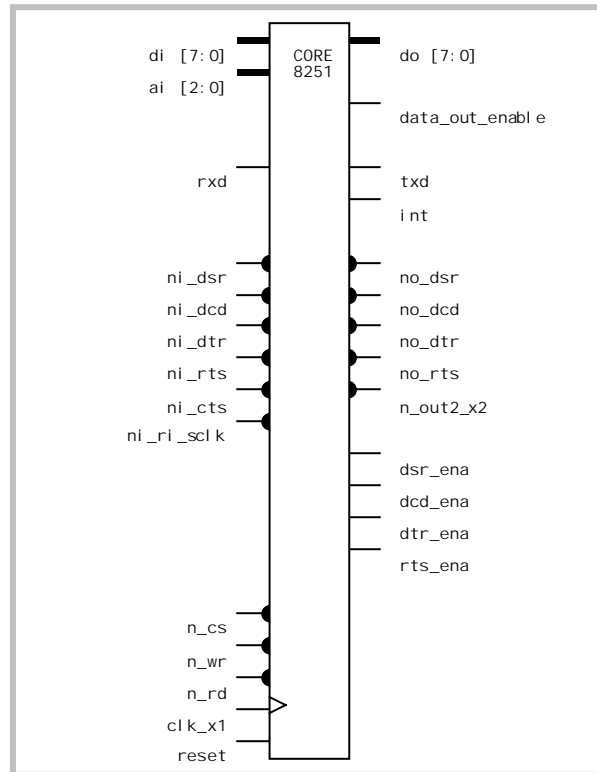


Figure 3

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Pin Description

Shell	Core	Type	Description
d7		in/out	data bit 7
d6		in/out	data bit 6
d5		in/out	data bit 5
d4		in/out	data bit 4
d3		in/out	data bit 3
d2		in/out	data bit 2
d1		in/out	data bit 1
d0		in/out	data bit 0
	do [7:0]	out	data bus output
	di [7:0]	in	data bus input
	data_out_enable	out	read <output> enable for data bus
a2		in	register selects (address bit 2)
a1		in	register selects (address bit 1)
a0		in	register selects (address bit 0)
	a [2:0]	in	register selects (address bus)
n_cs	n_cs	in	<not> chip select
n_wr	n_wr	in	<not> write strobe
n_rd	n_rd	in	<not> read strobe
int	int	out	interrupt
clk_x1	clk_x1	in	master clock
reset	reset	in	reset
rx	rx	in	serial receive data
tx	tx	out	serial transmit data
n_cts	ni_cts	in	<not> clear to send
n_dcd_clk_n_out1	no_dcd	out	<not> data carrier detect
	ni_dcd	in	<not>
	dcd_ena	out	<not>
n_r_clk	ni_r_clk	in	<not> ring indicator
n_dsr_ta_n_out0	no_dsr	out	<not> data set ready
	ni_dsr	in	<not>
	dsr_ena	out	<not>
n_rts	no_rts	out	<not> request to send
	ni_rts	in	<not>
	rts_ena	out	<not>
n_dtr_tb	no_dtr	out	<not> data terminal ready
	ni_dtr	in	<not>
	dtr_ena	out	<not>
n_out2_x2	n_out2_x2	out	<not> programmable output 2

table 1

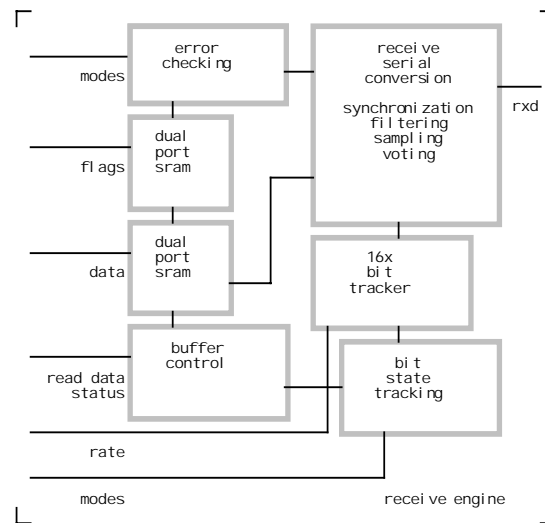
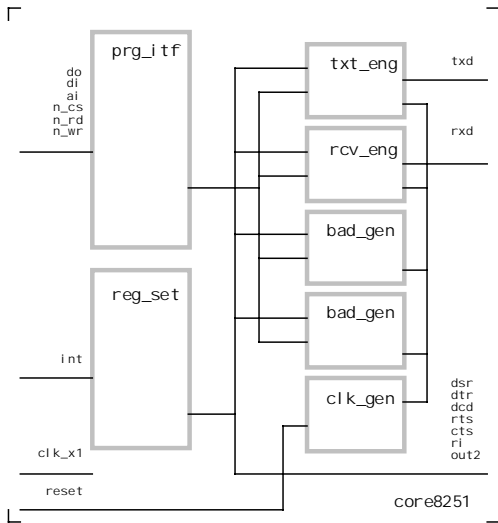
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Description

The VCM8251 is a synthesizable RTL core model and test bench for implementing a UART function compatible with the 82510 UART. It is partitioned into several

functional sub-sections. These are the prg_itf, reg_set, txt_eng, rcv_eng, clk_gen, and bad_gen modules.



figures 4a, 4b

Functional Blocks

The VCM8251 UART is partitioned into a core logic model and a shell model which contains bi-directional buffers. The core logic models contain only unidirectional signals. Figure 4a shows the functional blocks and their functional interconnects. The prg_itf module handles the data and control transfers between the internal registers, and the programming interface. The incoming control strobes, address selects, and data are all synchronized in this module. The reg_set is the register set for the line and modem, control and status registers. The reg_set also generates the

interrupt for the program interface. The bad_gen is the baud rate generator and timer functions. It provides the baud rate clock for transmit and receive operations. It is a programmable periodic counter. The txt_eng and rcv_eng are the transmit and receive engines for serial communications. These modules contain the memory buffers used for multiple data transfers. The memory is accessed just like most static memory. There is a pointer to the location, and controls for reading and writing the data. The functions in the receive block are shown in figure 4b.

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Programming Interface

The prg_itf functional block interfaces the internal registers to the programming (peripheral) bus. The incoming strobes and address are synchronized to the clock, (clk_x1). To write to an internal register, the address, (ai), chip select, (n_cs), and write strobe, (n_wr), must be active for 2 rising edges of the clock, plus the setup and hold time required by the implementation, (silicon target dependent). Recovery time between any two back to back accesses is at least one rising edge of the clock plus the implementation dependent setup and hold time. The read data bytes are assembled in this block. The write data and address are clocked and stabilized and internal read, write, post read and post write strobes are generated here. The post read and write

strobes are used to update status due to programming activity. An example of this is an update of the read pointer to the read buffer when a received character is read off of the top of this buffer. Figure 5 shows the timing for the programming interface for two register accesses, a read, and then a write, with the 1x clock option selected. This figure shows the fastest access possible. Note that the read data is not guaranteed until the second rising clock edge during the read strobe. Also, the width of the internal post read and post write signals are dependent on the input signals strobes (n_rd and n_wr) having sufficient setup to the rising edge of the clock, to provide adequate pulse width for these internal strobes.

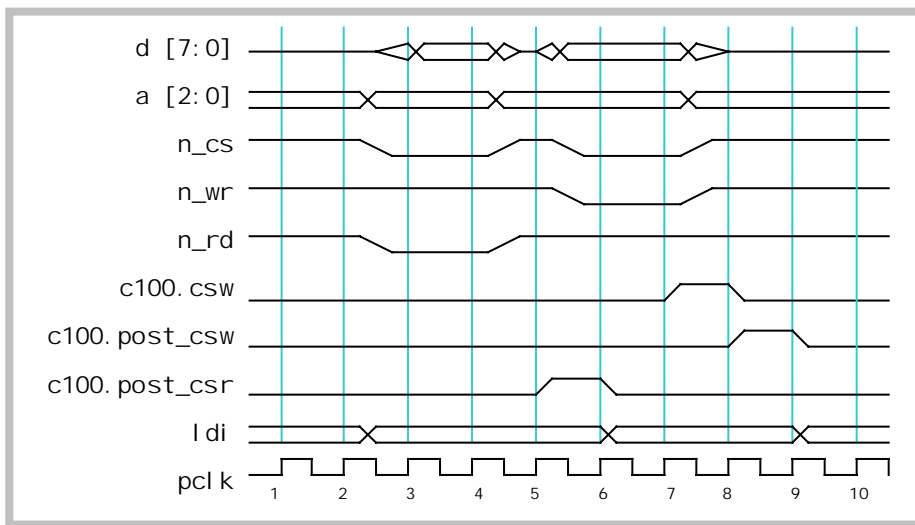


Figure 5

Register Set

The reg_set functional block contains most of the registers in the UART. This includes status, data transmit options, interrupt, configuration, and control registers. These registers are contained in one of 4 banks. Selection of banks 0 to 3 is accomplished by writing to the GIR register bits 6 and 5. This GIR register is available for access in all 4 banks, at the same address location.

Register bank 0 is compatible with the 16450 defined register set.
Register bank 1 provides an alternate operational register set for controlling the UART serial communications and for modem operations.
Register bank 2 provides detailed serial communications configuration registers.
Register bank 3 provides modem and clock configuration register access.

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These register banks are shown in tables 4 through 7 below.

The registers are considered static, except for changes in status due to incoming and outgoing characters, changes due to interrupt generation, and changes in status due to register access via the programming interface. The transmit buffered data, (tbd) receive buffered data, (rbd) and receive flags, (rxf) registers are in the transmit (txt_eng) and receive (rcv_eng) functional blocks respectively.

Clock Generation

The clk_gen clock generation circuit generates the reset for the internal registers, counters and state machines. This reset is either the reset input pin, or the result of the software reset, (icm[4]). It also generated the internal system clock which is selected via the hardware strapping option. This internal system clock can be either a 2x (divide master clock (clk_x1) by 2) or the master clock itself. The other strapping option is the oscillator or crystal support. The hardware strapping options works with the hardware reset ('reset' input pin), but not the software reset.

Baud Generation

The bad_gen contains the baud rate counter, which also can act as a programmable timer. There are two of these modules in the UART. Each functional block is identical. Use of the timer can result in the generation of an interrupt.

Transmit Engine

The txt_eng functional block contains the 16x bit timer, the character state machine, the data buffer and flag buffer, the buffer control logic, status generation logic, parity generation, and character serial conversion logic.

Receive Engine

The rcv_eng functional block contains all the logic to receive serial data characters, and

reliably convert the to parallel characters for the parallel programming interface. This involves several steps. The serial data is synchronized, glitches are filtered out, and the result is sampled (either 3 or 7 clocks). The sampling is a process of majority voting whereby if there are more marks than spaces, a '1' will be written into the appropriate register bit location. If not, then a '0' will be written into that bit location. When the stop bit is reached, the character is written into the read data buffer (if enabled). Likewise, the received character flags are written into a flag buffer for full status reporting at the parallel programming interface.

Automatic Transfer Modes

The transmitter can be enabled and disabled via register control bits. It can also be automatically controlled via hardware to transmit characters when the n_cts signal pin.

Diagnostic Functions

The local loopback mode 'shortcuts' the serial transmit output to the serial receive input. The serial transmit output signal pin is held at '1' to avoid transmitting characters during this diagnostic mode. There is also a remote echo mode which immediately returns the received serial bit to the serial transmit signal.

Noise Detection

The receive logic can detect noise on the serial receive input. A glitch of 1 clock duration will be ignored, but a signal change which spans more the 2 rising clock edges will be considered noise. If this noise falls in the sampling window, then it is reported on the status flags for that character.

Ulan Address Mode

The UART supports the Ulan address mode. In this mode, two address registers are compared with incoming characters, and if the address indicator is active, then an address compare is detected, and reported.

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Nine Bit Mode

An optional ninth bit can be added to the character. This bit is included in parity calculations.

Parity Options

The optional parity function checks selected parity on the incoming character. This includes 5, 6, 7, 8, 9, and Ulan address character configurations. Parity can be configured to be odd, even, set to '1', set to '0', or can reflect the software controlled register bit.

Timer Functions

The timer function is based on the periodic baud rate counter. There are two timers in the UART. When the timer is loaded, enabled, and triggered, the periodic baud counter will count down from the loaded value to result in an interrupt, if enabled.

Interrupt Features

Interrupts can be generated from 6 main sources. These are timer interrupts, transmitter buffer empty, transmit register empty, received character, receive errors, and modem status interrupts. Three of these main sources have their own sources for these interrupts. The timer interrupt can be generated by timer A or timer B. The modem status has 4 modem bits which are monitored for a change in state. Each of these 4 signals can result in an interrupt. The receive status has 8 possible sources.

Address and Character Recognition

The UART can recognize characters which are equal to either address register, or equal

to either ASCII or EBCDIC control character ranges. These options are programmable.

Serial Re-Synchronization

An edge detected on the serial input bit stream can re-synchronize the 16x bit timing counter. The synchronized, filtered version of the serial input is used for this function.

Serial Data Sampling

The serial input bit stream can be sampled with either 7 or 3 of the 16x clocks. A majority voting scheme is employed in these windows.

Stop Bit Length Options

Stop bit lengths from .75 to 2 can be selected.

Serial Error Detection

The receiver can detect the absence of a stop bit, (framing error), parity errors, overrun errors, and a break indication.

Clocking Options

There are several clock options. The internal baud generation can reflect the master clock (clk_x1) signal input pin), the internal sysclk (master clock divided by 2), or the external sclk signal input (n_ri_sclk). If the external clock is selected, the receive bit timing counter is not used. If not, the 16x bit timing counter is used.

Signal Pinout Options

There are several signal pins which have more than 1 possible function. These are software selectable via the pmd register.

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Option Selection via Constants

Several functional options can be selected by programming constants. Once

synthesized, these are no longer options, but are fixed.

Option	Block	Description
<i>p_early_write</i>	prg_itf	If set to 1, this constant will generate the internal register write strobe after detection, (and filtering) of the external write strobe. If set to 0, the internal write strobe will not be generated until the trailing edge of the external write strobe has been detected. The default for this constant is 0, (late write strobe selected).
<i>p_sys_clk_ena</i>	core8251	This parameter when set to 1, will use the internally generated sysclk to qualify and pace the read and write activity on the programming interface. This is mute if the 1x sysclk option is selected via the hardware strapping option. If the 2x sysclk option is used, then the interface will require twice as many clock edges for the read and write strobe active duration, and twice as many for the access recovery duration. If the constant is 0, the programming interface will work with the 3 clock minimum cycle, or the 6 clock cycle. The default for this constant is 0, (programming interface works with either fast or slow strobes and recovery).

table 2

Option Selection via Hardware Strapping Options

Several functional options can be selected at power up by hardware strapping options. These options are included in the synthesized hardware, so the user can

select the options when implementing silicon.

Option	Pin	Description
<i>sys clock rate</i>	dtr	If this signal pin is driven low during reset, then the internal sysclk reflects the master clock input (clk_x1). If not, then the internal sysclk will divide this master clock input by two, and functions like the baud rate, timer, transmit, and receive functions will operate with respect to this frequency. The programming interface will still operate strictly from the master clock input signal pin (clk_x1), unless the constant p_sys_clk_ena has been set to 1, in which case it will be paced by the internal divide by 2 system clock.
<i>osc or xtal</i>	rts	If this signal pin is driven low during reset, then a crystal oscillator configuration is supported on pins clk_x1 and out2_x2. In this mode, out2_x2 is an inverted form of the clk_x1 input. If it is not driven low, then an external oscillator is assumed to drive the master clock input, clk_x1. In this mode, the out_x2 signal pin is either the internal system clock, or out2 (inverted), which is a programmable output reflecting mcr[3]. In this mode, the output is selected via a software (pmd register).

table 3

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The register set

Register Bank 0:

REG	D L A B	B A N K	A D D R	OP	7	6	5	4	3	2	1	0	R S T
TBD	0	0	0	W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	--
RBD	0	0	0	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	--
BAL	1	0	0	RW	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	02
BAH	1	0	1	RW	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	00
GER	0	0	1	RW	0	0	Timer Int ena	Xmitr Int ena	Modem Int ena	Rcvr Int ena	Chr Xmit Int ena	Chr Rcvd Int ena	00
GIR	-	-	2	RW	0	Bank Select Bit 1	Bank Select Bit 0	0	Active Int bit 2	Active Int bit 1	Active Int bit 0	Int Pend	01
LCR	-	0	3	RW	dl ab	Set Break	Pari ty Mode Bit 2	Pari ty Mode Bit 1	Pari ty Mode Bit 0	StopBit Length Bit 0	Chr Length Bit 1	Chr Length Bit 0	00
MCR	-	0	4	RW	0	0	OUT 0	Loop back	OUT 2	OUT 1	RTS	DTR	00
LSR	-	0	5	RW	0	Xmit ter Empty	Xmit Buffer Empty	Break Detect	Fram ing Error Detect	Pari ty Error Detect	Overrun Error Detect	Chr Recei vd	60
MSR	-	0	6	RW	DCD	RI	DSR	CTS	DCD Del ta	RI 1-0 Del ta	DSR Del ta	CTS Del ta	00
ACRO	-	0	7	RW	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	00

table 4

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Register Bank 1:

REG	D L A B	B A N K	A D D R	OP	7	6	5	4	3	2	1	0	® R S T
TBD	-	1	0	W									--
RBD	-	1	0	R									--
TXF	-	1	1	W	Address Marker	Software Pari ty bi t	Data Bi t 9	0	0	0	0	0	--
RXF	-	1	1	R	-	Recei ve Chr OK	Recei ve Chr Noi sy	Recei ve Pari ty Error	A/C Chr Recei vd	Break Fl ag	Frami ng Error Recei vd	Data Bi t 9	--
GIR	-	-	2	RW									01
TMCR	-	1	3	W	0	0	Gate B	Gate A	0	0	Start Ti mer B	Start Ti mer A	--
TMST	-	1	3	R	-	-	Gate B	Gate A	-	-	Ti mer B Expi red	Ti mer A Expi red	30
MCR	-	1	4	W									00
FLR	-	1	4	R	-	Recei ve Buffer Level 2	Recei ve Buffer Level 1	Recei ve Buffer Level 0	-	Xmi t Buffer Level 2	Xmi t Buffer Level 1	Xmi t Buffer Level 0	00
RCM	-	1	5	W	Recei ver Enabl e	Recei vr Di sabl e	Reset Recei vr	Fl ush Recei ve Buffer	Lock Recei ve Buffer	Unl ock Recei ve Buffer	0	0	--
RST	-	1	5	R	A/C Chr Recei ved	A/C Chr Matched	Break End Detectd	Break Detectd	Frami ng Error Detectd	Pari ty Error Detectd	Overrun Detectd	Chr Recei vd	00
TCM	-	1	6	W	0	0	0	0	Reset Xmi tter	Fl ush Xmi tter Buffer	Xmi tter Enabl e	Xmi tter Buffer Di sabl e	--
MSR	-	1	6	R									00
ICM	-	1	7	W	0	0	0	Software Reset	Manual Int Ack	Status Cl ear	Reservd	0	--
GSR	-	1	7	R	-	-	Ti mer Int	Xmi tter Int	Modem Int	Recei vr Int	Xmi tter Buffer Int	Recei vr Buffer Int	12

table 5

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Register Bank 2:

REG	D L A B	B A N K	A D D R	OP	7	6	5	4	3	2	1	0	R S T
-NA-	-	2	0	--									--
FMD	-	2	1	RW	0	0	Recei vr Buffer Level 1	Recei vr Buffer Level 0	0	0	Xmi ttr Buffer Level 1	Xmi ttr Buffer Level 0	00
GIR	-	-	2	RW									01
TMD	-	2	3	RW	Error Echo Di sabl e	Control Chr Echo Di sabl e	9 Bit Mode Enabl e	Xmi t Mode Bit 1	Xmi t Mode Bit 0	Softw are Pari ty Mode ena	Stop Length Bit 2	Stop Length Bit 1	00
IMD	-	2	4	RW	0	0	0	0	Int Ack Mode	Recei ve Buffer Depth	Ul an Addr Mode Enabl e	Loop Back, Not Echo Mode	0c
ACR1	-	2	5	RW	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	00
RIE	-	2	6	RW	A/C Chr Recei vd Int Ena	A/C Chr Match ed Int Ena	Break End Detect d Int Ena	Break Detect d Int Ena	Frami ng Error Detect d Int Ena	Pari ty Error Detect d Int Ena	Over run Detect d Int Ena	0	1e
RMD	-	2	7	RW	A/C Chr Mode Bit 1	A/C Chr Mode Bit 0	DI I Di sabl e	Samp l ing Wi ndow Si ze	Start Bit Sampl e Enabl e	0	0	0	00

table 6

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Register Bank 3:

REG	D L A B	B A N K	A D D R	OP	7	6	5	4	3	2	1	0	RST
CLCF	0	3	0	RW	Recei vr Cl ock Mode	Recei vr Cl ock Source	Xmi ttr Cl ock Mode	Xmi ttr Cl ock Source	0	0	0	0	00
BACF	0	3	1	RW	0	BRGA Cl ock Source	0	0	0	BRGA Mode	0	0	00
BBL	1	3	0	RW	Bi t 7	Bi t 6	Bi t 5	Bi t 4	Bi t 3	Bi t 2	Bi t 1	Bi t 0	04
BBH	1	3	1	RW	Bi t 7	Bi t 6	Bi t 5	Bi t 4	Bi t 3	Bi t 2	Bi t 1	Bi t 0	05
GIR	-	-	2	RW									01
BBCF	-	3	3	RW	BRGB Cl ock Source Bi t 1	BRGB Cl ock Source Bi t 0	0	0	0	BRGB Mode	0	0	84
PMD	-	3	4	RW	DCD I nput Enabl e	DCD Functn Select	DSR I nput Enabl e	DSR Functn Select	RI Functn Select	DTR Functn Select	0	0	fc
MI E	-	3	5	RW	0	0	0	0	DCD Del ta Int Ena	RI 1-0 Del ta Int Ena	DSR Del ta Int Ena	CTS Del ta Int Ena	0f
TMI E	-	3	6	RW	0	0	0	0	0	0	TimerB Int Ena	TimerA Int Ena	00
-na-	-	3	7	--									--

table 7

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