



Macrocad Development Inc. VCM1013 Synthesizable UART Model

Description:

The VCM 1013 model from Macrocad is a synthesizable behavior HDL for creating an 16450 compatible UART function. Implementation is made easy for both FPGAs and ASICs. Synchronous design and small module size assures worry free synthesis. Well commented code provides insight into operations. Bi-directional signals are contained in the buffer (shell) level, the core contains unidirectional signals only.

Features:

- ? Synthesizable RTL HDL code
- ? Modular design provides flexibility
- ? Synchronous design
- ? Well commented code for clarity
- ? Test bench is included
- ? Available in Verilog and VHDL versions
- ? Approx. 2kgates (asic gates)
- ? Designed *by* hardware engineers *for* hardware engineers
- ? 16450 Compatible

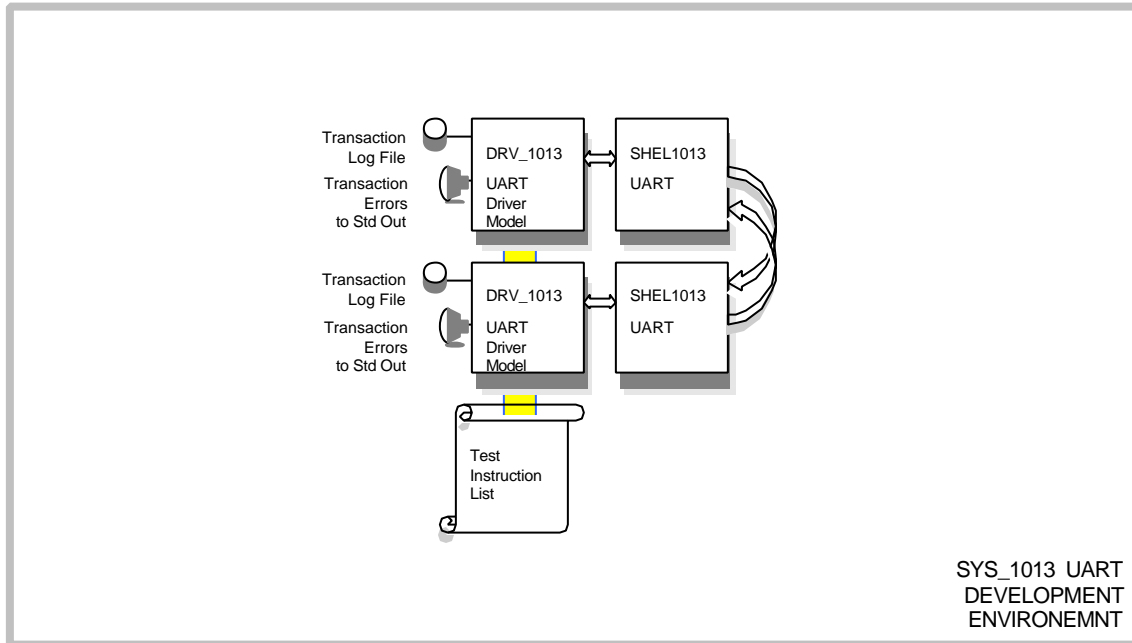


Figure 1

Figure 1 shows the development environment for the UART bus.

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Architecture

MacroCAD's VCM 1013 is a synthesizable 16450 compatible behavior model. This model provides the system designer with a drop in UART function. This model is functionally partitioned to provide the most flexibility for various ASIC and FPGA implementations. The IO buffer shell level

contains the only bi-directional signals in the model. The functional units are all contained in the core level. The core function model also contains debug features which display internal states during serial data transactions.

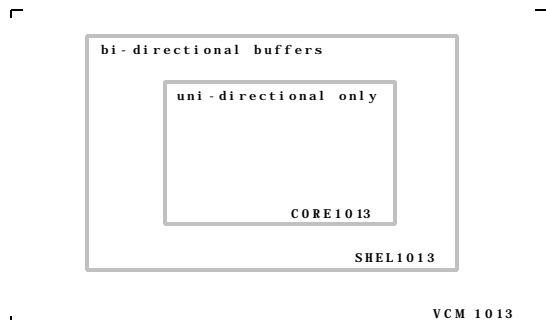


Figure 2

Core Pins

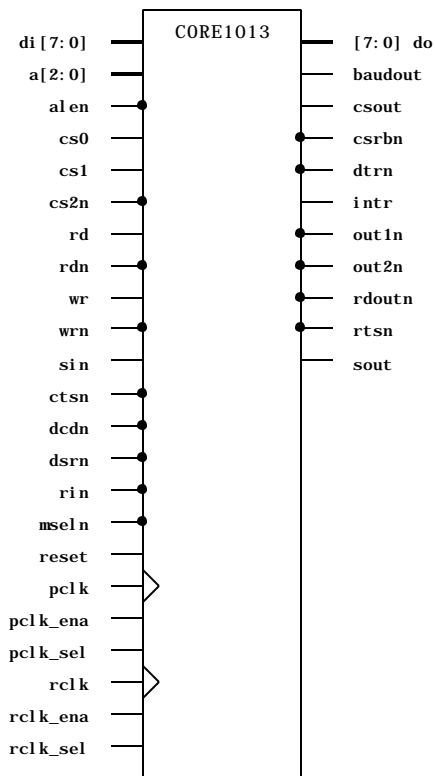


Figure 3

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Pin Description

Shell	Core	Type	Description
DB7		Bi-direct	Programming Data bit 7
DB6		Bi-direct	Programming Data bit 6
DB5		Bi-direct	Programming Data bit 5
DB4		Bi-direct	Programming Data bit 4
DB3		Bi-direct	Programming Data bit 3
DB2		Bi-direct	Programming Data bit 2
DB1		Bi-direct	Programming Data bit 1
DB0		Bi-direct	Programming Data bit 0
	DO [7:0]	Out	Programming Data bus output
	DI [7:0]	In	Programming Data bus input
	CSRBN	Out	read enable for data bus <not>
A2		In	Programming register selects (address bit 2)
A1		In	Programming register selects (address bit 1)
A0		In	Programming register selects (address bit 0)
	A [2:0]	In	Programming register selects (address bus)
ALEB	ALEN	In	Address latch enable <not>
CS0	CS0	In	Chip select 0
CS1	CS1	In	Chip select 1
CS2B	CS2N	In	Chip select 2 <not>
PCLK	PCLK	In	Programming clock <master clock>
XIN	PCLK_ENA	In	Enable for baud counter
CLK_SEL	PCLK_SEL	In	Baud clock select
RCLK	RCLK	In	Serial receive clock
	RCLK_ENA	In	Receive clock enable
	RCLK_SEL	In	Receive clock select
CTSB	CTSN	In	Clear to send - modem <not>
DCDB	DCDN	In	Data carrier detect - modem <not>
DSRB	DSRN	In	Data set ready - modem <not>
MSEL	MSELN	In	For test purposes, should be tied high
RD	RD	In	Programming read enable
WR	WR	In	Programming write enable
RDB	RDN	In	Programming read enable <not>
WRB	WRN	In	Programming write enable <not>
RESET	RESET	In	Reset
CI B	RIN	In	Ring indicator <not>
SIN	SIN	In	Serial receive data in
TRIN		In	Tri-state override <not> <for test only>
BAUDOUT	BAUDOUT	Out	Baud rate <x 16> output
CSOUT	CSOUT	Out	Chip select
DTRB	DTRN	Out	Data terminal ready <not>
INTRPT	INTR	Out	Interrupt
OUT1B	OUT1N	Out	Programmable output 1 <not>
OUT2B	OUT2N	Out	Programmable output 2 <not>
DDIS	RDOUTN	Out	Data bus output enable
RTSB	RTSN	Out	Request to send <not>
SOUT	SOUT	Out	Serial data stream transmit output
XOUT		Out	Reflects XIN input <not>

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Functional Blocks

MacroCAD's VCM 1013 is broken into several functional sub-sections. These are the PRG_ITF, REG_SET, INT_CTL, TXT_ENG, RCV_ENG, and BAD_GEN modules. The PRG_ITF module handles the data and control transfers between the internal registers, and the programming interface. The incoming control strobes, address selects, and data are all synchronized in this module. The REG_SET is the register set for the line

and modem, control and status registers. The scratch register and logic for the modem control is in this module also. The BAD_GEN is the baud rate generation engine. It provides the baud rate clock for transmit and receive operations. It is a programmable periodic counter. The INT_CTL generates the interrupt for the program interface. The TXT_ENG and RCV_ENG are the transmit and receive engines for serial communications.

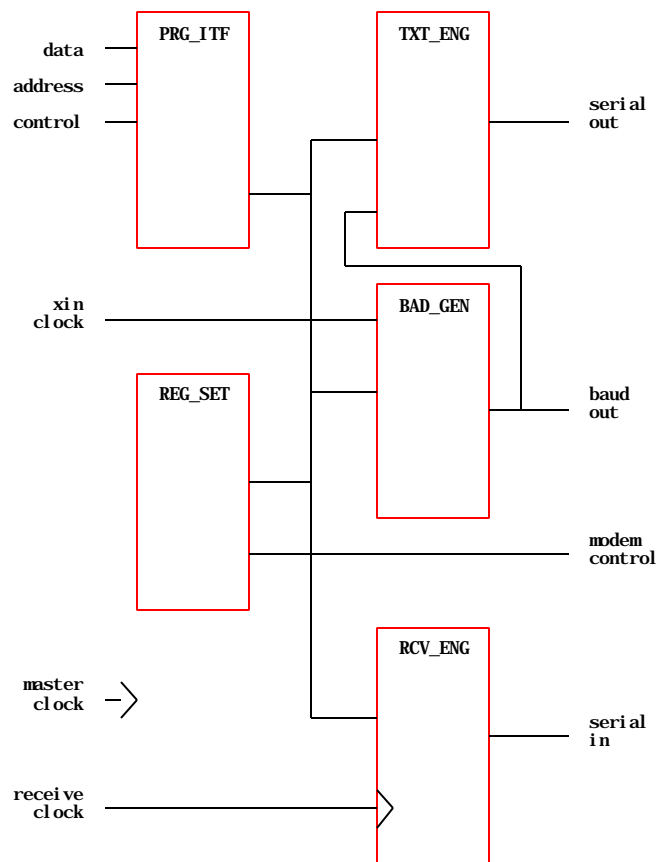


figure 4

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Register Address Map

ADDR:	DLAB:	OP:	BIT:	DESCRIPTION:	MODULE:
0	0	Wo	7:0	Transmit data register	txt_eng
0	0	Ro	7:0	Receive data register	rcv_eng
0	1	R/W	7:0	Baud rate register - low byte	bad_gen
1	0	R/W	3:0	Interrupt enable register	int_ctl
1	1	R/W	7:0	Baud rate register - hi byte	bad_gen
2	-	Ro	7:0	Interrupt ID register	int_ctl
3	-	R/W	7:0	Line control register	reg_set
4	-	R/W	4:0	Modem control register	reg_set
5	-	R/W	7:0	Line status register	reg_set
6	-	R/W	7:0	Modem status register	reg_set
7	-	R/W	7:0	Scratch register - user register	reg_set

table 2

Access to the registers is accomplished by 3 address pins and 3 chip select lines. Two strobes are used to read and write the internal registers. Bit 7 in the Line Control Register (DLAB = 1) is used to select the two baud rate registers when the part is being set up for operation. When in operation (DLAB = 0) the transmit, receive, and interrupt enable registers are enabled instead of the baud rate registers. The registers are written to on the rising edge of the PCLK (program clock) if the proper address has selected it. The two status registers

(Line and Modem) can be written in this same way. The bits in these registers are also written when the internal transmit and receive state machines reach certain conditions. The operational access to internal registers is synchronous, although asynchronous strobes can be used if there is at least two rising clock edges within the strobe active time. Read access is required to follow these same requirements not due to data bus output delays, but due to status register updates due to reading of the status registers.

Register Bit Descriptions

ADDR:	REGISTER:	OP:	DESCRIPTION:	@RESET
A DLAB				
000 0	RHR	R	Receive Holding register	
000 0	THR	W	Transmit Holding register	
001 0	IER	R/W	Interrupt enable register	00
			7:4 always 0000	
			3: Modem Status	
			2: Receiver line status	
			1: Transmitter Holding register empty	
			0: Receive Data Available	
000 1	DLL	R/W	Baud divisor register (LEAST)	
001 1	DLM	R/W	Baud divisor register (MOST)	
010 -	IIR	R	Interrupt ID register	01
			7:4 RESERVED	
			3:1 Interrupt ID[2:0]	
			0: 0 = Interrupt Pending	
011 -	LCR	R/W	Line control register	00
			7: Divisor latch access enable (DLAB)	
			6: Set break	
			5: Stick parity	
			4: Even parity select	
			3: Parity enable	
			2: Stop bit	
			1:0 Word length select	
100 -	MCR	R/W	Modem control register	00
			7:5 always 000	
			4: Loop	
			3: OUT2	

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101 -	LSR	R/W	2: OUT1 1: Request to send 0: Data terminal ready Line status register 7: reserved 6: Transmitter Empty 5: Transmitter Holding Register Empty 4: Break interrupt 3: Framing error 2: Parity error 1: Overrun 0: Data ready	60
110 -	MSR	R/W	Modem status register 7: Data carrier detect 6: Ring indicator 5: Data set ready 4: Clear to send 3: Delta data carrier detect 2: Trailing edge ring indicator 1: Delta data set ready 0: Delta clear to send	x0
111 -	SCR	R/W	Scratch register	

table 3

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Functional Blocks

The VCM1013 UART is partitioned into a core logic model and a shell model which contains bi-directional buffers only. The core logic models contain only unidirectional signals. The core contains the UART features and functions found in the industry standard 16450 UART. All shell level output and bi-direct pins can be tri-stated with the TRIN signal pin. (This is a test feature.) The VCM1013 core function is partitioned into 6 modules.

1 PRG_ITF : Program interface module

This module handles the interface to the parallel IO programming pins. It synchronizes data and provides synchronous register write enables. The UART registers are inputs to this module. They are multiplexed into the output data bus for reading.

2 REG_SET : Register set module

This module contains the registers which control and provide status to the parallel programming interface. The Line Control and Status, Modem Control and Status, and Scratch registers are contained in this module.

3 TXT_ENG : Transmit engine module

This module contains the serial transmit engine. It includes the data path, serial conversion, parity generation and the state machine for serial transmission of data. It serializes the data in the transmit register. A counter is used to divide the baud clock by 16 to achieve the serial bit stream controlled by a state machine. A loop back feature is included for diagnostics.

4 RCV_ENG : Receive engine module

The receive module receives data from the serial interface, and presents it as a byte for reading by the programming interface. It includes the state machine and serial to parallel conversion as well as parity checking. Odd and even parity are supported, and are selectable in the Line Control Register. This module also checks for framing errors. It samples and synchronizes the incoming serial data stream.

5 BAD_GEN : Baud generation engine module

This module generates the baud rate clock for the serial interface. There is a 16 bit modulo binary counter contained in this module. This module contains a 16 bit baud rate generation register. These are accessed as two byte registers. If the baud rate register is written to the value 0x00001 the counter is disabled, and the CX frequency rate is the frequency which is applied to the transmit and receive circuits. Writing either baud rate register will reload the counter to the baud rate register values. The counter is clocked by the PCLK which is program interface clock. The CX clock is sampled and the counter runs at this clock's rate.

6 INT_CTL : Interrupt control module

The interrupt control module generates an interrupt (INTR signal pin). Interrupts can result from the modem, transmit, and receive sources. This module prioritizes interrupts and generates them depending on the interrupt enable register. It will also clear the interrupts if the appropriate clear procedure is applied to the model.

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Block Functional Descriptions

1 PRG_ITF

This module converts the CS1, CS0, ALEN, WR, WRN, RD, RDN, and A[2:0] inputs into the appropriate strobes and gate signals to write and read the CORE1013 registers. This module also contains the logic to determine which mode the part will operate in based on the logic state of the MSELN input at reset.

In mode 0 operation the CS1, CS0, and A[2:0] inputs are latched when ALEN is de-asserted and flow through when asserted. The WR (asserted active high) and WRN (asserted active low) inputs are or'ed together; when either is asserted a write operation is selected. The RD (asserted active high) and RDN (asserted active low) inputs are or'ed together; when either is asserted a read operation is selected.

NOTE: The logic does not prohibit the simultaneous selection of both a read and write cycle.

If the MSELN option input is sampled low at reset time (mode 1) address and CS0 input are not latched, requiring that they be stable throughout the read or write cycle. In mode 1 the CS1 input need not be asserted for read or write cycles, and the state of the CS1 input can be read from the scratch pad register bit 0. Also, in mode 1 the ALEN input must be de-asserted to enable read data output buffers and the SOUT output buffer.

2 REG_SET

The REG_SET (register set) module is comprised of the Line Control, Line Status, Modem Control, Modem Status, and Scratch Registers.

2.1 LCR - Line control register

The LCR register provides the control bits necessary to control both the transmitter

and receiver sections. Bit 7 of this register is the divisor latch access bit, which must be set to one to enable access to the Divisor registers.

2.2 LSR - Line status register

This register reflects the state of serial transfers. It indicates receive errors, (overrun, framing and parity errors), receive break, receive character and the status of the transmit buffer.

- 7: reserved
- 6: Transmit serial transfer NOT active
- 5: Transmit buffer empty and no transfer in process
- 4: Break interrupt detected
- 3: Framing error detected
- 2: Parity error detected
- 1: Overrun in receive buffer detected
- 0: Data received <at least 1 buffer location>

2.3 MCR - Modem control register

This register controls the interface with the MODEM or data set.

- 0: DTR This bit controls the Data Terminal Ready output. The register bit gets inverted and drives the DTRn output.
- 1: RTS This bit controls the Request To Send output. The register bit gets inverted and drives the RTSn output.
- 2: OUT1 This bit controls the Output 1 output. The register bit gets inverted and drives the OUT1n output.
- 3: OUT2 This bit controls the Output 2 output. The register bit gets inverted and drives the OUT2n output.
- 4: LOOP When this bit is set to one the macro goes into loop-back mode. In loop-back mode the SOUT bit is forced to one and the transmit output register is internally directed to the receiver logic replacing the SIN input. The modem outputs are

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forced into their inactive state (1) and the outputs from the Modem control register are internally directed to the modem inputs as follows:

DTR -> CTS,
RTS -> DSR,
OUT1 -> RI, and
OUT2 -> DSR.

2.4 MSR - Modem status register

This register indicates the state of the modem control and status bits.

- 7: DCD data carrier detect input signal
- 6: RI ring indicator input signal
- 5: DSR data set ready input signal
- 4: CTS clear to send input signal
- 3: DDCD delta - change in DCD detected since last read of MSR
- 2: TERI trail - trailing edge of RI detected since last read of MSR
- 1: DDSR delta - change in DSR detected since last read of MSR
- 0: DCTS delta - change in CTS detected since last read of MSR

2.5 SCR - Scratch register

This 8 bit write/read register does not control any of the UART functions. When in operating mode 1 (see section 4.1) bit 0 reflects the state of the CS1 input rather than bit 0 of the scratch register.

3 TXT_ENG

The TXSTATE module controls the loading and shifting of the external transmit shift register module. The serial data output from the transmit shift register module gets clocked into the output and parity generator registers within the TXSTATE module.

The module has dual serial outputs to enable the loop-back mode of operation. When in loop-back mode the SOUT module output will be held at a logic 1 and the transmit serial output data

stream gets diverted to the RXD output replacing the SIN data stream. The RXD output drives the receiver logic.

The module contains the by 16 divisor for the BAUDOUT signal necessary to control the output bit rate. The TXSTATE state machine runs off of the BAUDOUT signal divided by 16. The state machine handles the different transmitter operating modes (eg. word length, parity, and start/stop bits).

3.1 THR - Transmit holding register

This register holds the data for the transmitter to send. The value from this register get serially transferred to the serial interface pin starting with the lowest order bit of the selected location. Bit 5 of the LSR register indicates whether the buffer currently has a value loaded waiting to transfer to the serial output pin.

4 RCV_ENG

The RXSTATE module controls the loading of the external receive capture latch, and receive buffer latch. A read from the receive holding register latches the data from the receive buffer latch in the receive holding register. The RXSTATE module contains two state machines, a by 16 receive clock divisor to generate the bit rate clock from the RCLK input, and a receive parity sum register.

The RXSYNC sub-module contains the state machine which controls the by 16 receive clock divisor, break detection logic, and framing error detection logic. The RXSYNC module disables the clock to the RXSTATE main state machine until a start bit has been detected.

The main state machine of the RXSTATE module captures the appropriate bit into the receive capture latch from the RXD input. After capturing the entire word in the capture latch the contents are transferred to the receive buffer latch.

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4.1 RHR - Receiver holding register

This register is the latched data from the receive buffer.

5 BAD_GEN

The BAD_GEN (baud rate generation) module contains the divisor registers and clock divider network for the BAUDOUT output. The BAUDOUT frequency will be the XIN clock rate divide by the value in the divisor registers. The BAUDOUT signal determines the transmitted serial rate of data transmission. Data will be transmitted at a rate of one bit for every 16 BAUDOUT cycles. Frequently the BAUDOUT output gets tied to the RCLK input to be used in the receiver section also.

A divisor of one will generate a time delayed and buffered version of the XIN input. A divisor of two generates a 50% duty cycle half rate version of the XIN input. When the divisor(DIV) is 3 or greater the BAUDOUT will be low for two XIN clock cycles and high for DIV-2 XIN clock cycles. A divisor(DIV) of 0 is modified to a divisor of 16 by the logic.

5.1 DLL - Baud rate generator register (least).

This register holds the 8 least significant bits of the divisor value. The DLAB bit must be set to one to enable write/read access to this register.

5.2 DLM - Baud rate generator register (most).

This register holds the 8 most significant bits of the divisor value. The DLAB bit must be set to one to enable write/read access to this register.

6 INT_CTL

This module enables the four types of UART interrupts. Each interrupt can individually assert the interrupt (INTR)

output. When a respective interrupt enable bit is set to a logic 1 the interrupt is enabled.

The INT_CTL module contains the interrupt enable register and gates which mask or pass the respective interrupts. The outputs from the INT_CTL module feed a priority encoder which sets the appropriate bits in the Interrupt Identification register and also drives the INTR output to a logic 1 when an enabled interrupt is pending.

6.1 IER - Interrupt enable register

This register allows for individual enabling of interrupts.

7: 4 RESERVED

- 3: Enable modem status change interrupt
- 2: Enable receive error detect interrupt
- 1: Enable transmitter empty interrupt
- 0: Enable data received interrupt

6.2 IIR - Interrupt ID register

When read this register returns the encoded value of the highest priority interrupt pending. Bit 0 indicates whether an enabled interrupt is currently pending. This register is the latched outputs of the interrupt priority encoder. The data is latched during a read operation.

7: 4 RESERVED

- 3: 1 Interrupt ID
 - 011 : receive error detected < highest priority >
 - 110 : character timeout
 - 010 : data received
 - 001 : transmitter empty
 - 000 : modem status change - lowest priority
- 0: Interrupt inactive < interrupt pin inverted >

Clock Considerations

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The PCLK is the main clock for the VCM1013 design. It is assumed that this clock runs at least 4X of the CX (xin) frequency. If a smaller differential is needed, then the CX signal should be tied

high. The model will then use the PCLK for operations without the CX qualifier. The programming interface and register access ignores the CX clock.

Test Configuration

The VCM1013 UART is tested by a test behavior module which exercise the model and its various functions. Two UARTs are instantiated in the test. One is configured for receive, and the other is configured for transmit. There are also

two test drivers instantiated. There are two handshaking signals used as a way to communicate between the two instantiated test drivers. In this way, the two tests can keep in sync.

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