

Macrocad Development Inc. VCM 1011 Synthesizable Interrupt Controller Model

Description:

Macrocad's VCM 1011 model is a synthesizable behavior HDL for creating an 8259 compatible Interrupt Controller function. The parallel IO programming interface is synchronous to a single clock edge, avoiding silicon based delay chains. Implementations are made easy for both FPGAs and ASICs. Synchronous design and small module size assures worry free synthesis. Interrupt channels are individually selectable between edge and level with an 8 bit select bus. Well commented code provides insight into operations. Test vectors and a test behavior support model are included.

Features:

- ◇ Synthesizable RTL HDL code
- ◇ Modular design provides flexibility
- ◇ Synchronous design
- ◇ Well commented code for clarity
- ◇ Test behavior is included
- ◇ Available in Verilog and VHDL versions
- ◇ Approx. 1.5k gates (asic gates)
- ◇ Designed *by* hardware engineers *for* hardware engineers
- ◇ Fully compatible with the 8259
- ◇ 2 or 3 cycle interrupt acknowledge
- ◇ Individually selectable trigger options

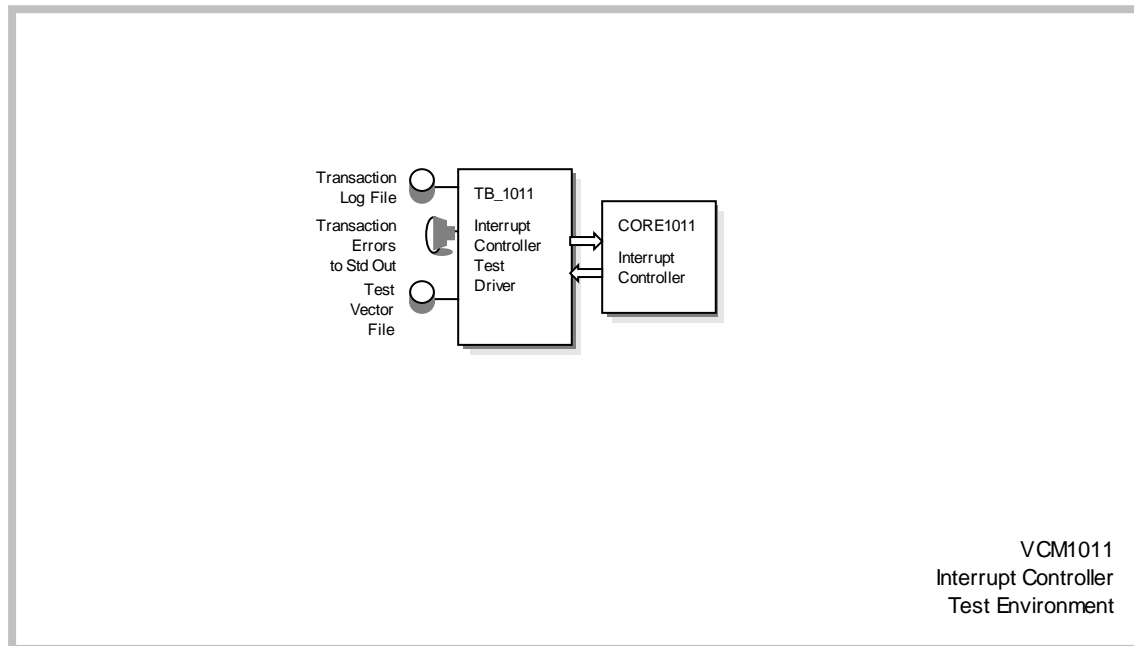


Figure 1

Figure 1 shows the test environment for the VCM1011 Interrupt Controller model.

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Architecture

The VCM 1011 Interrupt Controller model is functionally partitioned to provide the most flexibility for various ASIC and FPGA implementations. The IO buffer shell level contains the only bi-directional signals in the

model. The functional units are all contained in the core level. At this level, various functional units are connected to provide specific capabilities for the overall Interrupt operations.

Core Pins

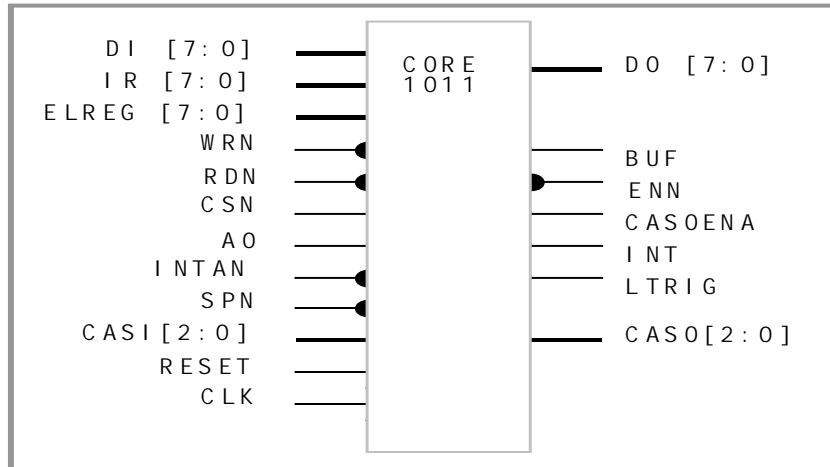


figure 2

PINOUT FOR VCM 1011 INTERRUPT CONTROLLER MODULE			
		Inputs	
<i>INTAN</i>		IO read for interrupt acknowledge	1
<i>WRN</i>		IO write for programming registers	1
<i>RDN</i>		IO read for programming registers	1
<i>CSN</i>		Chip select	1
<i>AO</i>		Address bit for register selection	1
<i>RESET</i>		Reset	1
<i>CLK</i>		Programming clock - positive edge	1
<i>ELREGENA</i>		Enable of ELREG - IR edge selection	1
<i>ELREG</i>	[7:0]	Individual edge or level selects	8
<i>IR</i>	[7:0]	Interrupt inputs	8
<i>SPN</i>		Input section of external bi-direct	1
<i>CASI</i>	[2:0]	Slave Program mode	3
<i>DI</i>	[7:0]	CAS inputs for slave mode operation	8
		Data	8
		TOTAL INPUTS	36
		Outputs	
<i>INT</i>		Interrupt output	1
<i>ENN</i>		Enable data bus outputs	1
<i>CASOENA</i>		Enable cas bus outputs	1
<i>BUF</i>		Initialization control word 4 bit 3	1
<i>LTRIG</i>		Initialization control word 1 bit 3	1
<i>CASO</i>	[2:0]	Output section of external bi-direct	3
<i>DO</i>	[7:0]	CAS outputs for slave mode operation	8
		Data	8
		TOTAL OUTPUTS	16
		TOTAL SIGNALS	52

table 1

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Register Set

ADDR 0	DATA 4, 3	OCWB 1, 0	Init RDY	REGISTER	OP	DESCRIPTION
0	1-	--		ICW1	W	Initialization Control Word 1
1	--	--	0	ICW2	W	Initialization Control Word 2
1	--	--	0	ICW3	W	Initialization Control Word 3
1	--	--	0	ICW4	W	Initialization Control Word 4
1	--	--	1	OCW1	W	Operational Control Word 1
0	00	--	1	OCW2	W	Operational Control Word 2
0	01	--	1	OCW3	W	Operational Control Word 3
1	--	--	1	IRMR	R	Interrupt Mask Register
0	--	11	1	INSR	R	In Service Register
0	--	10	1	IRRR	R	Interrupt Request Register

table 2

Register Mapping

Output Signal	Module	Description
MASKED	IRSERV	OCW1 Interrupt Mask Register
RI AEOI	RDWR8259	OCW2 Rotate In Automatic End of Interrupt Mode
SPECM	RDWR8259	OCW3 Special Masked Mode
ISRSEL	RDWR8259	OCW3 Selects ISR or IRR register for reading
POLLMODE	RDWR8259	OCW3 Selects Poll mode
ADDRESS	INITCTL	ICW1 Address bits for Interrupt Acknowledge
LTIM	INITCTL	ICW1 Level Trigger Mode
ADI 4	INITCTL	ICW1 Address call interval of 4 (8 when 1'b0)
CASCADE	INITCTL	ICW1 Selects Single or multiple device config
IC4	INITCTL	ICW1 determines whether ICW4 is needed or not
ADDRESS	VEC3CTL	ICW2 Address bits for Interrupt Acknowledge
SLAVEID	IRSERV	ICW3 Slave ID register slave[2:0] master[7:0]
SFNM	INTACTL	ICW4 Special Fully Nested Mode
BUF	INTACTL	ICW4 Buffered mode
MASTER	INTACTL	ICW4 Only significant in Buffered mode
AEOI	INTACTL	ICW4 Automatic End of Interrupt
I8086	INTACTL	ICW4 Selects I8086 mode or MCS80_85 mode
ISR	IRSERV	ISR In Service Register
IRR	IRSERV	IRR Interrupt Request Register
PRIORITY	IRSERV	PRIORREG Interrupt Priority Register

table 3

Functional Blocks

After the PIC has been initialized (indicated by PICRDY==1'b1) writes are decoded as Operation Command Words(OCW). Note that after initialized the device may be re/initialized via a write with A0==1'b0 and D[4]==1'b1.

OCW1:

Selected when A0==1'b1. OCW1 is the interrupt mask register. The interrupt mask register can be found in the IRSERV module. The mask bits which are set (1) block (force inactive) the outputs from the Interrupt Request register which feed the IR priority mask circuit. When enabled by the

Special Mask Mode (SPECM) register, the mask bits are applied to the In Service register prior to feeding the IS priority mask circuit. The SPECM bit is set and cleared via OCW3. The IMR(latch) is not written until after either the chip select or write inputs are de/asserted.

A0	D7	D6	D5	D4	D3	D2	D1	D0
1	M7	M6	M5	M4	M3	M2	M1	M0

OCW2:

Selected when A0==1'b0 and D[4:3]==2'b00. OCW2 controls how and/or when the priority register gets modified at

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End Of Interrupt(EOI). Automatic End Of Interrupt (AEOI) is enabled or disabled during initialization. Rotation in AEOI mode is controlled via the RAEOI register in this module. The RAEOI register may be set or cleared through writes to OCW2.

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	R	SL	EOI	0	0	L2	L1	L0
0	0	1	Non/Specific EOI command (NSEOI)					
0	1	1	Specific EOI command (SEOI)					
1	0	1	Rotate on Non/Specific EOI command					
1	0	0	Rotate In Automatic EOI mode (set)					
0	0	0	Rotate In Automatic EOI mode (clear)					
1	1	1	Rotate on Specific EOI command					
1	1	0	Set Priority command					
0	1	0	NO OPERATION					

L2/L0 are only significant for Rotate On Specific EOI (RSEOI) and the Set Priority commands and specify the affected IR level. The SETPRIORN output signal will be asserted for one CLK cycle after de/assertion of either of the chip select or write inputs for RSEOI, RNSEOI, and Set Priority commands.

OCW3:

Selected when A0==1'b0 and D[4:3]==2'b01. The ISRSEL,POLLMODE, and SPECMM registers are controlled via writes to OCW3 independent of one another.

ISRSEL:

Writes to OCW3 set or clear the In Service Select (ISRSEL) register, which controls which register (ISR or IRR) will be returned on reads when A0==1'b0. The ISRSEL register receives the value of D[0] on writes to OCW3 WHEN D[1]==1'b1.

POLLMODE:

Polled mode operation is enabled on writes to OCW3 with D[2]==1'b1. The POLLMODE register receives the value of D[2] on writes to OCW3. The POLLMODE register will get cleared AFTER the next read from the device (A0==1'bx). When the POLLMODE register is one the next read of the device asserts the POLLRDN signal which provides a software mechanism for generating an INTA pulse.

SPECMM:

Writes to OCW3 may also set or reset the Special Mask Mode (SPECMM). The Special Mask Mode register enables or disables the effect of the interrupt mask register on the ISR register outputs which feed the ISR priority mask logic. Thus, by disabling the highest priority level in service, software can re/enable lower priority interrupts which may also be in service. The SPECMM register receives the value of D[5] on writes to OCW3 WHEN D[6]==1'b1.

Functional Description

The VCM1011 core functionality is subdivided into a hierarchy of modules:

MODULE DEFINITIONS:

Programming interface sections:

- 1 RDWR8259 - read write programming interface
- 2 VEC2CTL - vector generation for 2 inta cycle mode
- 3 VEC3CTL - vector generation for 3 inta cycle mode
- 4 INITCTL - initialization control word access control

Interrupt in service section:

- 5 IRSERV - interrupt service registers - contains:

- interrupt capture register, priority register
- mask register, and in service register

Interrupt response section:
6 INTACTRL - interrupt control - response to interrupts

1 The RDWR8259 module is the interface between the internal register set and the programming interface. The asynchronous delays in the original 8259 are replaced by a synchronous interface. Several registers are write only, and some are addressed by a combination of address and data bits. The

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RDWR8259 module also contains the OCW2, and OCW3 registers.

The RDWR8259 module generates the appropriate read and write pulses to initialize the PIC modes(WRICW1N, INITCLRN, DECICW1N). It also generates the write/read pulses for the interrupt mask register(READIMRN), generates the read pulses for the In Service Register(READISRN), and Interrupt Request register(READIRRN). This module generates the interrupt acknowledge pulse required to ack interrupts in the polled mode of PIC operation (POLLMODEN and POLLRDN).

The ENN(active low) and ENA(active high) outputs from the RDWR8259 module are the tri-state control signals for the data outputs from the core8259 module when connected to an external tri-state bus.

The RDWR8259 module latches the single address bit A0 on writes or reads. A0 is latched when both the chip select(CSN) and the read(RDN) or write(WRN) inputs are asserted and remains latched for three positive edges of the clock(CLK) after the de/assertion of any one of the chip select, write, or read inputs.

The RDWR8259 module latches the eight data bit DI[7:0] inputs on writes. The data is latched whenever either of the chip select or the write input are de/asserted (latch is open when both chip select and write input are asserted).

2 The VEC2CTL module provides interrupt vectors during interrupt acknowledge cycles. The VEC2CTL module determines the data driven onto the DO lines during the second INTA pulse.

3 The VEC3CTL module provides interrupt vectors during interrupt acknowledge cycles. This module contains the address bits for this type of interrupt acknowledge cycle,

ICW2. The VEC3CTL module determines the data driven onto the DO lines during the third INTA pulse in MCS/80 mode or on a polled mode read.

4 The INITCTL module controls access to the initialization sequence, and contains the ICW1, Initialization Control Word 1. The INITCTL module contains the four bit initialization state machine which generates the Initialization Command Word(ICW) write strobes for ICW2, ICW3, and ICW4. The ICW1 register is maintained within this module. The state machine bit PICRDY is an output from the module and indicates that the initialization sequence has been completed when PICRDY==1'b1.

The state machine is clocked on the rising edge of the clock when the WRPLSN signal is low, which will be asserted after either the chip select or write inputs to the device are de/asserted. The WRPLSN input is guaranteed to have a minimum width of one CLK period. The CASCADE and IC4 register (latch) values are written on the ICW1 write.

5 The IRSERV module contains the IR, IS, MASK, SLAVEID (ICW3), and PRIORITY registers. This module processes the incoming interrupts, asserts the INT signal, and resolves which of the interrupt inputs has the highest priority. At acknowledge time (INTA or POLLED MODE command) the state of the IRR register is frozen (latch closed) and the highest priority level In service bit gets set and its IRR bit gets cleared.

6 The INTACTL module contains the ICW4 register. This module creates the access signals to the other modules as a result of the various interrupt acknowledge cycles which can occur. It must be aware of the mode that the controller is in, and understand the inta sequences to manage the setting and resetting of register bits in the controller.

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