

Macrocad Development Inc.

VCM1010 Synthesizable Counter Timer Model

Description:

The VCM 1010 model from Macrocad is a synthesizable behavior HDL for creating an 8254 compatible Counter Timer function. Implementation is made easy for both FPGAs and ASICs. The parallel IO programming interface is synchronous to a single clock edge, avoiding silicon based delay chains. Synchronous design and small module size assures worry free synthesis. Well commented code provides insight into operations. Bi-directional signals are contained in the buffer (shell) level, the core contains unidirectional signals only.

Features:

- ◇ Synthesizable RTL HDL code
- ◇ Modular design provides flexibility
- ◇ Synchronous design
- ◇ Well commented code for clarity
- ◇ Test behavior is included
- ◇ Available in Verilog and VHDL versions
- ◇ Approx. 2.5k gates (asic gates)
- ◇ Designed *by* hardware engineers *for* hardware engineers
- ◇ Six counting modes
- ◇ Programmable output and trigger options

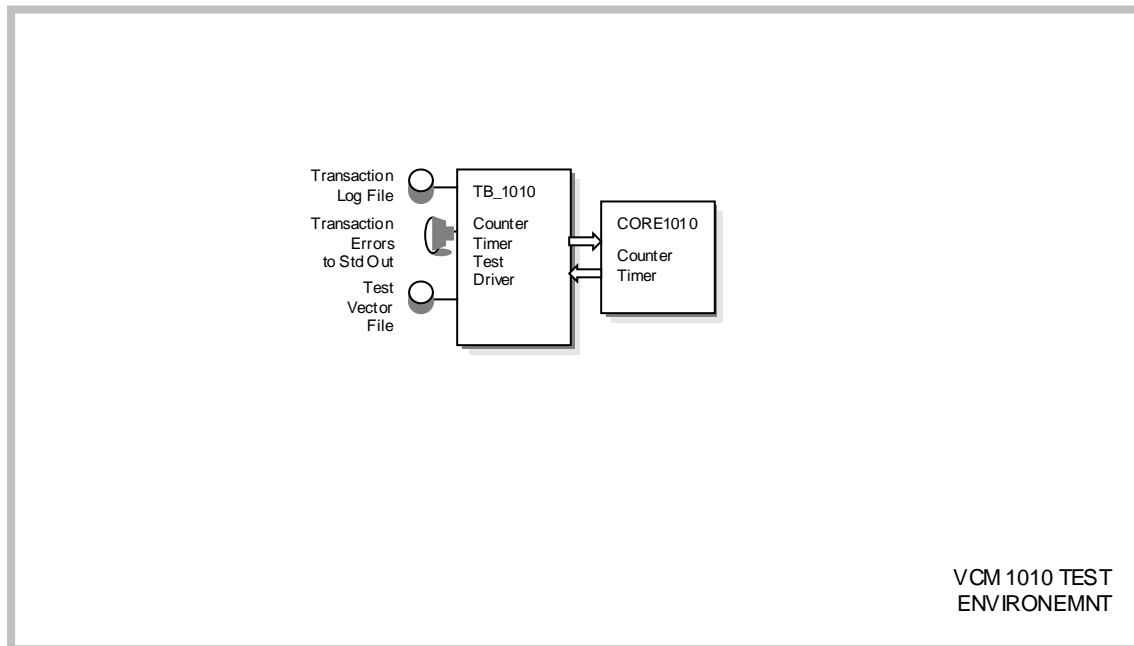


Figure 1

Figure 1 shows the test environment for the Counter Timer bus.

VCM 1010



Architecture

The VCM 1010 Counter Timer model is functionally partitioned to provide the most flexibility for various ASIC and FPGA implementations. The IO buffer shell level contains the only bi-directional signals in the

model. The functional units are all contained in the core level. At this level, various functional units are connected to provide specific capabilities for the overall Interrupt operations.

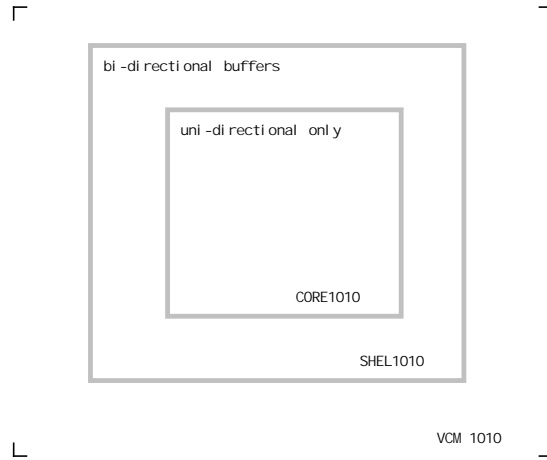


Figure 2

Core Pins

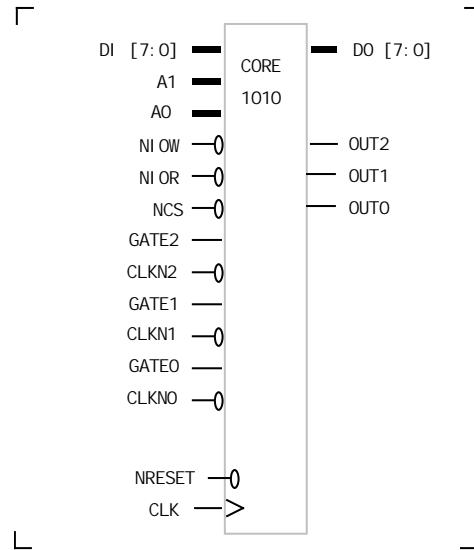


Figure 3

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Pin Description

SIGNAL PINS FOR CORE1010		
Outputs:		
<i>DO</i>	8	Programming data output
<i>OUT2</i>	1	Counter 2 output
<i>OUT1</i>	1	Counter 1 output
<i>OUT0</i>	1	Counter 0 output
SUBTOTAL:	11	Inputs
Inputs:		
<i>DI</i>	8	Programming data input
<i>A1</i>	1	Address 1 input
<i>AO</i>	1	Address 0 input
<i>NCS</i>	1	Chip select
<i>NIOW</i>	1	IO write strobe
<i>NIOR</i>	1	IO read strobe
<i>CLKN2</i>	1	Counter 2 clock input
<i>GATE2</i>	1	Counter 2 gate input
<i>CLKN1</i>	1	Counter 1 clock input
<i>GATE1</i>	1	Counter 1 gate input
<i>CLKN0</i>	1	Counter 0 clock input
<i>GATE0</i>	1	Counter 0 gate input
<i>NRESET</i>	1	Global reset
<i>CLK</i>	1	Programming interface clock
SUBTOTAL:	21	Outputs
TOTAL:	32	Signals

table 1

Functional Blocks:

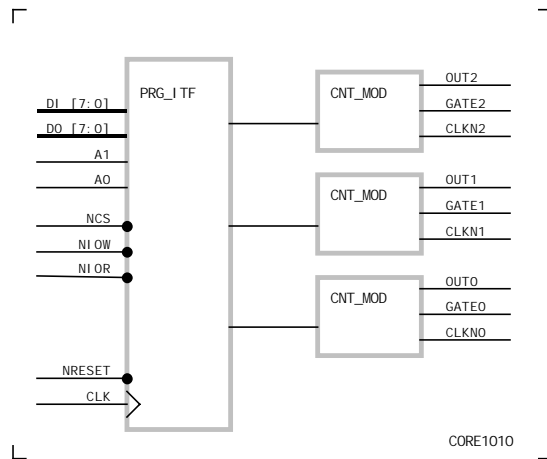


figure 4

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Register Set

Register Address Map:

REGISTER ACCESS			
Address:	Register:	Op:	Description:
00	CT0	R/W	Counter 0
01	CT1	R/W	Counter 1
10	CT2	R/W	Counter 2
11	CTRL	W o	Control Word
11		R	NA - (returns '0xFF')

table 2

Register Bit Descriptions:

REGISTER:	BITS:	NAME:	DESCRIPTION:
Control Word	7: 6	SC [1: 0]	Select Counter = 11: Read Back Command = 10: Counter 2 = 01: Counter 1 = 00: Counter 0
	5: 4	RW [1: 0]	Read Write Operation = 11: Least significant byte then most significant byte = 10: Least significant byte only = 01: Least significant byte only = 00: Counter Latch
	3: 1	MODE [2: 0]	Counting mode = 111: mode 3 = 110: mode 2 = 101: mode 5 = 100: mode 4 = 011: mode 3 = 010: mode 2 = 001: mode 1 = 000: mode 0
	0	BCD	Binary Coded Decimal = 1: BCD = 0: Binary
Status Word	7	OUT	Counter's Output signal
	6	NULL	Counter's Null Condition
	5: 4	RW [1: 0]	Read Write Operation = 11: Least significant byte then most significant byte = 10: Least significant byte only = 01: Least significant byte only = 00: Counter Latch
	3: 1	MODE [2: 0]	Counting mode = 111: mode 3 = 110: mode 2 = 101: mode 5 = 100: mode 4 = 011: mode 3 = 010: mode 2 = 001: mode 1 = 000: mode 0
	0	BCD	Binary Coded Decimal = 1: BCD = 0: Binary

table 3

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Control / Status Register Description

Control Word:

SC	<p>Select counter: These two bits determine access to the counters' mode registers. SC = 00: Selects counter 0's mode register. SC = 01: Selects counter 1's mode register. SC = 10: Selects counter 2's mode register. SC = 11: Selects the readback command, described below. Each counter's mode register has 6 bits, and they are defined as in the control word: RW[2:0], MODE[2:0], and BCD. Each counter could have a different mode of operation for counting, as well as for programming sequences and access. Read Back Command: When this command is executed, the remaining bits of the control word are redefined as follows: Bit 5: latch the counter's count value if this bit is equal to '0' Bit 4: latch the counter's status if this bit is equal to '0' Bit 3: select counter 2 Bit 2: select counter 1 Bit 1: select counter 0 Bit 0: not defined One or more counter may be selected for latch operations with this command. To read the status or count which has been latched by this command, read the appropriate counter's byte location as selected by the address bits. If both status and counter bytes are latched, then reading the counter will result in status being returned followed by the least, then the most significant bytes of the counter.</p>
RW	<p>Selected counter's Read write operation: RW = 00: Counter latch command, described below RW = 01: Access to the least significant byte RW = 10: Access to the most significant byte RW = 11: Access to the least significant byte followed by the most significant byte Counter Latch Command: When this command is executed, the output latch for the counter (selected by SC) will update. The contents of both bytes will be frozen so even though the counter continues to count, the output will remain stable for reading the counter value at the time of the counter latch command.</p>
MODE	<p>Selected counter's mode of counting: There are 6 modes of counter operation. MODE0: INTERRUPT ON TERMINAL COUNT OUT is high, until the counter reaches '0'. The counter will then stop, and the OUT signal is high until programming the counter. MODE1: HARDWARE RETRI GGÉRABLE ONE SHOT OUT is high until the GATE signal goes high, and will remain low until the counter has reached '0'. The Gate signal going high also loads the counter to provide a fixed period for the OUT signal to be low. Since the counter is programmable, the period is programmable. MODE2: RATE GENERATOR The OUT signal will be high until the counter reaches '0'. It will be low for one clock, and this will reload the counter which is periodic. MODE3: SQUARE WAVE GENERATOR The OUT signal has the attributes of a square wave. The counter reloads when it reaches '0', thus the counter is periodic. MODE4: SOFTWARE TRIGGERED STROBE The OUT signal will be high until the counter reaches '0'. It will then be low for 1 clock. The counter can be reprogrammed to restart the sequence. MODE5: HARDWARE TRIGGERED STROBE (RETRI GGÉRABLE) The OUT signal will be high until the counter reaches '0'. It will be low for one clock, then high again. The counter is enabled to count by the GATE signal going high.</p>
BCD	<p>Selected counter's Decimal or binary counting: Each counter can be programmed to binary (BCD = 0) or decimal counting modes, (BCD = 1).</p>

table 4

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Status Word:

Out	Selected counter's output signal state: This reflects the state of the selected counter's "OUT" signal.
NULL	Selected counter's null state: This reflects the state of the counter with respect to null or the count of "0x0000". It will be null when some counting sequences have completed or reached terminal count, (see mode descriptions), or when programming a value into the counter has started, but not completed.
RW	Selected counter's Read write operation: See Control Word description
MODE	Selected counter's mode of counting: See Control Word description
BCD	Selected counter's Decimal or binary counting: See Control Word description

table 5

Functional Description

The VCM1010 counter timer consists of three identical 16 bit counters which count down from a programmed value to 0x0000. Each counter has a mode register, a status holding register, and count holding register, and an initial count register.

The counters can be programmed in a variety of ways. The counter has 6 modes providing various ways to count, and various ways for the OUT signal to operate. The counters are accessed in a byte mode only. There are provisions made to freeze the count holding register so that even though the counter continues to update, the count holding register is frozen for the programming interface to read. There are

status bits for each counter. These may also be put into a holding register so that they may be read back at a later time. Both counter bytes may be accessed sequentially with the low byte first followed by the high byte.

The counters operate in one of six different modes. These range from periodic (repetitive), to single event counting modes. They can make use of the external trigger via the GATE signal, or ignore it. Their OUT signals can be set to transition only at the terminal count, or at the time of enabling the counter. The modes of operation are described in the control word section.

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